

**Frequency Divider 1:64****SDA 2101****Bipolar IC  
MOS Handling**

Type	Ordering code	Package
SDA 2101	Q67000-A1753	P-DIP 8

The IC has been designed for application in TV receivers using frequency selection according to the frequency synthesis concept. It includes a preamplifier and an ECL divider with a dividing ratio of 1:64.

The frequency range extends up to 1 GHz.

- Few external components

**Maximum Ratings**

Supply voltage	$V_B$	6	V
Input voltage (UHF/VHF & reference) (peak-to-peak)	$V_i$	2.5	V
Divider outputs	$V_{q6}, V_{q7}$	0 to $V_S$	V
Junction temperature	$T_j$	150	°C
Storage temperature range	$T_{stg}$	-40 to 125	°C
Thermal resistance			
System-air	$R_{th SA}$	115	K/W
System-case	$R_{th SC}$	60	K/W

**Operating Range**

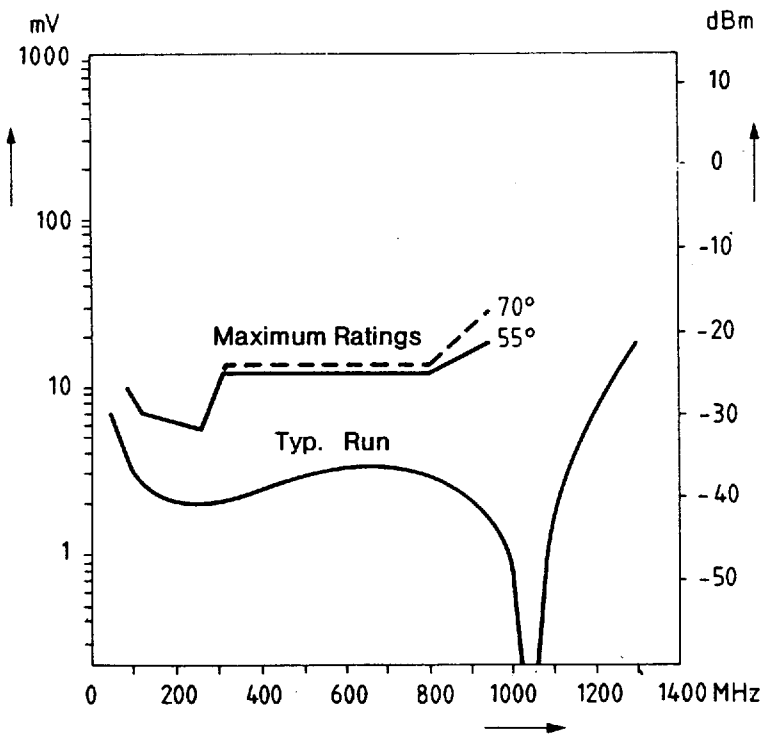
Supply voltage	$V_B$	4.7 to 5.5	V
Input frequency	$f_{i1}$	80 to 1000	MHz
Ambient temperature range (80 MHz to 950 MHz)	$T_A$	0 to 85	°C

**Characteristics**

$V_S = 5\text{ V}; T_A = 25\text{ }^\circ\text{C}$

	min	typ	max	Unit
Input level ("input sensitivity") $V_S = 4.7\text{ to }5.5\text{ V}; T_A = 0\text{ to }70\text{ }^\circ\text{C}$				
80 MHz	-27		3	dBm
120 MHz	-30		3	dBm
250 MHz	-32		3	dBm
300 MHz	-24		3	dBm
800 MHz	-24		3	dBm
950 MHz	-15		3	dBm
$V_S = 4.7\text{ to }5.5\text{ V}; T_A = 0\text{ to }55\text{ }^\circ\text{C}$				
800 MHz	-25			dBm
950 MHz	-21			dBm
$V_S = 4.7\text{ to }5.5\text{ V}; T_A = 0\text{ to }25\text{ }^\circ\text{C}$				
800 MHz	-27			dBm
950 MHz	-27			dBm
Current consumption		$I_B$	50	mA
Output voltage swing (peak-to-peak)	0.5	$V_6, V_7$	1.0	V
Output voltage "high"		$V_6, V_7$	$V_S$	V

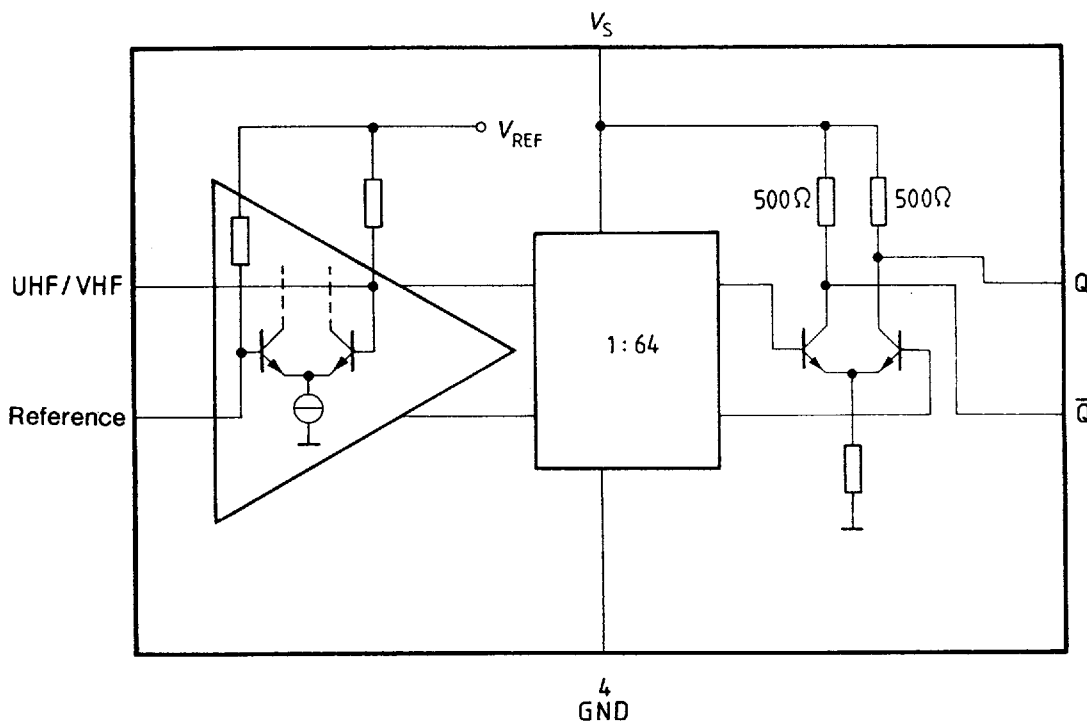
**Typical Input Sensitivity of the Divider**



### Circuit Description

The amplifier of the IC features a VHF/UHF input and a reference input. The reference input should be disabled by a capacitor with low series inductance. The divider of the component consists of several, status-controlled master-slave flipflops with a dividing ratio of 1:64. The divider output supplies a symmetrical ECL push-pull signal.

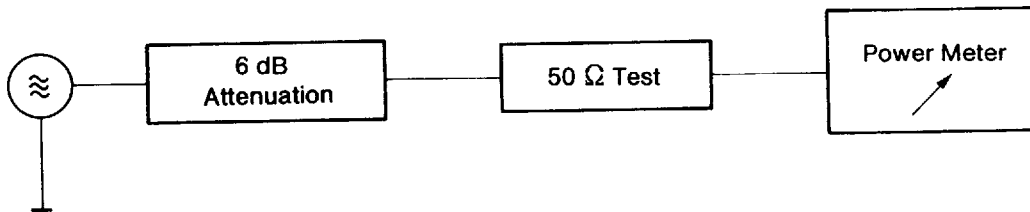
### Block Diagram



**Test and Measurement Circuit**

**Signal Generator**

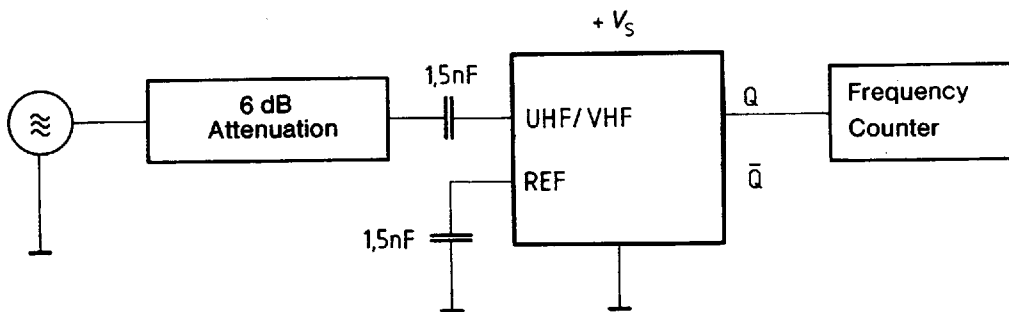
$Z_o = 50 \Omega$



**Test Circuit 1: Calibration of Signal Generator**

**Signal Generator**

$Z_o = 50 \Omega$



**Test Circuit 2: Measurement of Input Sensitivity**

**Pin Definitions**

Pin	Function
1	N.C.
2	UHF/VHF signal input
3	Reference input
4	GND
5	N.C.
6	Divider output $\bar{Q}$
7	Divider output Q
8	Supply voltage +Vs